Remarks

Claim 1 is amended herein. Claims 1 - 32 are in the application, of which claims 14 - 32 were withdrawn as being directed to a nonelected invention. Accordingly, claims 1 - 13 are now under consideration.

Reconsideration of the application, as amended, is requested.

The points raised in the Office action will now be addressed.

Rejections under 35 U.S.C. § 102(b)

Claim 1 was rejected under 35 U.S.C. §102 as being anticipated by Massit *et al.* U.S. 5,373,189 ("Massit"). The Examiner repeated his assertions from the previous Office action:

> Massit discloses a multipackage module having a second package (4c) stacked over a first package (4b), each said package comprising a die (10c and 10b, respectively) attached to a substrate (6c and 6b, respectively), the second package substrate (6c) and the first package substrate (6b) being interconnected by wire bonding (13c), wherein the first package comprises a ball grid array package (10b with 11b, Fig. 1 and Cols. 4-5).

This rejection is traversed. Applicant, respectfully, disagrees with the Examiner's reading of Massit, in at least the following respect.

Massit nowhere suggests, much less describes, a ball grid array package. A multipackage module according the invention, in which the first package is a ball grid array package, is described in Applicant's specification (e.g., Paragraphs **[0068]** - **[0069]**) with reference to, for example, FIG. **5A**. The ball grid array package **400** includes a die attached to a substrate having circuitry in at least one metal layer, in which the circuitry includes bonding sites at the die attach side for electrical interconnection of the die with the substrate and for z-interconnection of the second package substrate and, in addition, bonding pads at the side of the substrate opposite the die attach side, for mounting the second level interconnection solder balls 418. Massit says nothing about second-level interconnection, or about any ball grid array on the side of the substrate opposite the die interconnect side.

Referring now to the Examiner's particular reference to Massit Fig. 1: the feature (10a) of Massit is a die (semiconductor chip). An interconnection network or array (8a) covers the upper surface of a support (6a) The die (chip) (10a) is connected to the interconnection network (8a) by

means of connections (11a) and (11a'). (Massit Col. 4, lines 15 - 20.) That is, Massit describes "flip chip" interconnection of the chip on a metallization on the substrate ("hybridization of the chip on the substrate" in Massit; See, e.g., Col. 5, lines 1 - 5). This has nothing to do with a ball grid array.

In response to these arguments, which were presented in Applicant's reply to the earlier Office action and which the Examiner deemed "not persuasive", the Examiner asserted:

> ... [A] ball grid array is merely an attachment structure which incorporates conductive balls to attach two elements such as substrate to substrate, chip to substrate or chip to chip. Massit does disclose "flip chip" bonding which incorporates the use of solder balls, therefore Massit discloses the limitation "wherein the first package comprises a ball grid array package". This interpretation of ball grid array structures is commonly known in the art of semiconductor technology. As evidence to support such teachings, but not relied upon for the rejection, please see the background section Col. 1, line: 50 – Col. 2, line: 15 of Quek et al. (US 6492726).

An array of interconnect balls may indeed be referred to as a "ball grid array", and flip chip attachment of a die to a substrate using an array of minute solder balls disposed on the surface of the flip chip that attaches to the substrate may be referred to as "ball grid array" flip chip interconnection. (This is the terminology Quek employs as one of several electrical connectors that may be employed for face-down mounting of the flip chip with a substrate; *See, e.g.*, Quek *et al.* U.S. 6,492,726 ["Quek"] Col. 1, line 50 - Col. 2, line 15.).

That is not where Applicant disagrees with the Examiner's reading of the art. Applicant maintains that a "ball grid array package" has interconnect solder balls attached (for example by solder reflow) to interconnection sites (such as bond pads) at the side of the substrate opposite the die attach side. The die may be interconnected with the substrate in any of a variety of ways. For example, a "ball grid array package" may have the die interconnected to the substrate by flip chip interconnection (and the flip chip interconnection may be, for example, by an array of minute balls on the active surface of the die -- the BGA interconnection mentioned by Quek) (*see, e.g.*, Applicant's FIG. 3, ¶ **[0021]** *et seq.*). Or, for example, a "ball grid array package" may have the die mounted active side upward, and electrically interconnected by wire bonds on the die attach side of the substrate (*see, e.g.*, Applicant's FIG. 1, ¶ **[0016]** *et seq.*). Similarly, a "ball grid array package" may have any of a variety of other die-to-substrate attachment means (such as, for example, "tab interconnection").

Quek describes BGA "Ball Grid Array" interconnection of the die with the substrate, and not all packages having BGA interconnection of the die with the substrate are "ball grid array packages"; flip chip package may be, for example, a land grid array package (*see, e.g.*, Quek Col. 4, lines 28 *et seq.*).

Accordingly, Massit does not disclose that the first package is a "ball grid array package", notwithstanding the fact that Massit shows "flip chip bonding which incorporated the use of solder balls".

Claim 1 is amended herein to recite that each package in the multipackage module includes a die attached to a first side of a substrate, and to recite, in place of "ball grid array package" that the first package also includes solder balls connected to bonding pads at a second side of the first package substrate. Accordingly the claim as amended includes a recitation that expressly distinguishes the meaning of "ball grid array package". This recitation substantially imports into the claim the meaning of "ball grid array package" as used in the specification and as understood in the art, and, accordingly, the amendment does not narrow the scope of the claim or of any element of it.

Accordingly, Massit does not describe all the features of Applicant's invention as claimed in claim 1 and, accordingly, the rejection of claim 1 as being anticipated by Massit should be withdrawn.

Claims 1 - 7 were rejected under 35 U.S.C. §102 as being anticipated by Takiar *et al.* U.S. 5,495,398 ("Takiar"). Again the Examiner merely reiterated his assertions from the previous Office action. As to claim 1, the Examiner asserted:

> Takiar discloses a multipackage module having a second package [(136 and 142, Fig. 7), (216 and 214, Fig. 11), (264 and 262, Fig. 14)] stacked over a first package [(138 and 140, Fig. 7),(212 and 218, Fig. 11), (264 and 260, Fig. 14)], each said package comprising a die [(140 and 136, Fig. 7), (216 and 212, Fig. 11), 264 and 260, Fig. 14)] attached to a substrate [(138 and 142, Fig. 7), (214 and 218, Fig. 11), (262 and 268, Fig. 14)], the second package substrate and the first package substrate being interconnected by wire bonding, wherein the first package comprises a ball grid array package (Figs. 1, 7, 11, 14 and Col. 4, lines: 35-65 and Col. 7, lines: 22-40 and Col. 9).

This rejection is again traversed; the Examiner has not addressed Applicant's arguments as presented in the reply to the previous Office action. Applicant disagrees with the Examiner's reading of Takiar, in at least the following respect.

Takiar nowhere suggests, much less describes, a ball grid array package. As explained above, a multipackage module according the invention, in which the first package is a ball grid array package, is described in Applicant's specification (e.g., Paragraphs **[0068] - [0069]**) with reference to, for example, FIG. **5A**. The ball grid array package **400** includes a die attached to a substrate having circuitry in at least one metal layer, in which the circuitry includes bonding sites at the die attach side for electrical interconnection of the die with the substrate and for z-interconnection of the second package substrate and, in addition, bonding pads at the side of the substrate opposite the die attach side, for mounting the second level interconnection solder balls **418**. Takiar says nothing about second-level interconnection, or about any ball grid array on the side of the substrate opposite the die interconnect side.

Referring now to the Examiner's particular reference to Takiar Figs. 1, 7, 11 and 14; and Col. 4, lines 35 - 65, Col. 7, lines 22 - 40 and Col. 9: These Figs. (and associated text) show various packages having die mounted on a "carrier", which includes leads by which interconnection of the package is made (e.g., leads (44), (46) in Takiar Fig. 1). This has nothing to do with a ball grid array. In fact, the Examiner has not shown where in Takiar there is any suggestion, much less any teaching, of an array of balls of any kind. (Still less is there any suggestion in Takiar of a "ball grid array package".)

Accordingly, Takiar does not describe all the features of Applicant's invention as claimed in claim 1.

Applicant does not agree in every particular with the Examiner's reasoning with reference to claims 2 - 7, but those claims all depend directly of indirectly from claim 1, and so the points need not be addressed here. Accordingly, the rejection of claims 1 - 7 as being anticipated by Takiar should be withdrawn.

Rejections under 35 U.S.C. § 103(a)

Claims 8 - 13 were rejected under 35 U.S.C. §103(a) for obviousness over Takiar in view of Chen *et al.* U.S. 6,472,741 ("Chen"). This rejection is traversed.

In response to Applicant's arguments in reply to the earlier Office action, the Examiner states that "Applicant also argues that there is no suggestion to combine the Chen reference with the Takiar reference." This is not well understood. Applicant argues as follows.

Takiar was applied as in the rejections under 35 U.S.C. § 102(b). The Examiner acknowledged that Takiar does not describe a heat spreader having a generally planar upper surface exposed at the top of the module. Chen is relied upon as teaching a heat spreader (claims 8 - 10) which, the Examiner argues, one could "realize ... as an electromagnetic shield ... since it is composed of metal."

This rejection is traversed. In view of the lack of any suggestion or teaching in Takiar of second package stacked over a first ball grid array package, it is not understood how any combination of Takiar with Chen makes Applicant's invention as claimed.

Even if there were a motivation to combine Chen with Takiar, no such combination makes Applicant's invention, because -- as explained above -- there is no teaching or suggestion in Takiar of a second package stacked over a ball grid array package.

Accordingly Applicant's invention as claimed is not taught or suggested by any combination of the cited patents and, accordingly, the rejections for obviousness should be withdrawn.

In view of the foregoing, all the claims now in the application are believed to be in condition for allowance, and action to that effect is respectfully requested

This Response is being filed within the first month following the three months' shortened statutory period set by the Examiner for response to the Office action and, accordingly, it is accompanied by a Petition for one month's extension of time and a fee or fee authorization therefor. In the event the Examiner may determine that additional fee[s] may be required in connection with the filing of this paper, petition is hereby made therefor, and the Commissioner is authorized to charge any additional fee (or to credit any overpayment) to Deposit Account No. 50-0869 (CPAC 1017-3).

Atty. Docket No. CPAC 1017-3
Appl. No. 10/632,568

PATENT

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

Reg No. 33,407

Bill Kennedy
Reg. No. 33,407

Haynes Beffel & Wolfeld LLP
P.O. Box 366
Half Moon Bay, CA 94019
Telephone: (650) 712-0340